In the Specification:

Paragraph beginning on page 1, line 20

One of the problems is that millions of personal computers have found their place in the home market. Today, PCs can be found in [approximately 43%] over 60% of all United States households, many of which have more than one computer networked, [and a full] while over 50% of United States teenagers own computers. Virtually every PC sold today is equipped with a modem, enabling communication with the outside world via commercial data networks and the Internet. Currently, people use their PCs to send and receive e-mail, to access online services, to participate in electronic commerce and to browse the Internet. The popularity of the Internet is such that there are [an estimated 50] over 100 million users around the globe. These figures indicate that in the past few years the personal computer has fueled a dramatic increase in data communications and the corresponding demands on the data networks that carry the traffic.

Paragraph beginning on page 1, line 30

The Internet serves as a good example of the increased demands that have been placed on data networks. At first, Internet access consisted of text only data transfers. Recently, with the popularity of the World Wide Web (WWW) and the construction of numerous sites with high quality content, coupled with the development of Internet browsers such as Mosaic, Netscape Navigator and Microsoft Internet Explorer, the use of graphics, audio, video and text has surged on the Internet. While graphics, audio and video make for a much more interesting way to view information as opposed to plain text, bandwidth consumption is significantly [more] higher. A simple background picture with accompanying text requires approximately 10 times the bandwidth needed by text alone. Real-time audio and streaming video typically need even more bandwidth. Because of the increased requirement for bandwidth, activities such as browsing home pages or downloading graphics, audio and video files can take a frustratingly long period of time. Considering that the multimedia rich World Wide Web accounts for more than one quarter of all Internet traffic, it is easy to see why the demand for bandwidth has outpaced the supply. In addition, the creative community is pushing the envelope by offering audio and full motion video on numerous sites to differentiate themselves from the millions of other sites competing for [maximum] user hits.

Paragraph beginning on page 4, line 32

[It] In accordance with the VDSL Draft Specification it is intended that the Tx and Rx SOC [signal] signals be used by the CPE to synchronize the transmission and reception of the data to and from VDSL modem. In the case of transporting Ethernet data over the VDSL facility, a problem arises, however, when attempting to [sync] synchronize Ethernet frames to VDSL frames. The problem with using these Tx and Rx SOC signals is that the VDSL frame [is] comprises a fixed number of bytes, e.g., 256 bytes, whereas the Ethernet frame may vary from 64 to 1518 bytes. Designing and implementing the circuitry, e.g., state machines, timing and framing circuits, etc., to perform the protocol matching, i.e., sync timing between Ethernet frames and VDSL frames is very complicated and hence expensive to implement.

Paragraph beginning on page 6, line 6

The VDSL facility transport system comprises an Ethernet to VDSL Customer Premises Equipment (CPE) [coupled to] in communication with a DSL Access Multiplexor (DSLAM) over a VDSL transport facility. The DSLAM is typically located at the curb or before the 'last mile' in a subscriber loop. The Ethernet to VDSL CPE functions to receive a 10BaseT Ethernet signal and encapsulate the Ethernet frame into a VDSL frame for transmission over the VDSL facility. Likewise, the Ethernet to VDSL CPE also functions to receive a VDSL signal, extract Ethernet frames therefrom and output them as standard 10BaseT Ethernet signals.

Paragraph beginning on page 11, line 22

A transport facility suitable for use with the present invention is the 10BaseS transport facility described in detail in U.S. [Application Serial] Patent No. [08/866,831 filed May 30, 1997] 6,088,368, entitled 'Ethernet Transport Facility Over Digital Subscriber Lines,' similarly assigned and incorporated herein by reference. A brief description of this transmission system is given below.

Paragraph beginning on page 15, line 25

In accordance with the IEEE 802.3 standard, Ethernet data is transmitted using Manchester coding whereby an idle character is transmitting using DC and [a] '0' and '1' characters are transmitted [having] with a transition half way through the symbol, the transition for a '0' being opposite that for '1'.

Paragraph beginning on page 17, line 3

The Ethernet encapsulation/extraction unit 52 will now be described in more detail. A block diagram illustrating the Ethernet encapsulation/extraction (EEE) unit of the present invention in

more detail is shown in Figure 8. Note that the EEE unit resides in both the CPE and [in] the DSLAM, [which together help constitute] both of which are part of the Ethernet over VDSL transport facility of the present invention. They also form a major portion of the 10BaseS system which the present invention may be used to construct as described hereinabove.

Paragraph beginning on page 17, line 18

The EEE unit performs several functions including interfacing the data signals from the Ethernet transceiver 50 (Figure 3). Note that the interface may comprise the seven wire Ethernet interface link provided by the Motorola MPC850 microprocessor. The EEE unit also interfaces to the VDSL transceiver that may comprise the Broadcom BCM6010 VDSL transceiver as described previously. In this case, the interface is via the Transport Independent Parallel Interface of the BCM6010. Control and management of the memory 120 so as to implement store and forward of Ethernet frames in the direction of both the VDSL transceiver and the Ethernet transceiver is also performed by the EEE unit.

Paragraph beginning on page 20, line 13

The Ethernet frame is transmitted over the VDSL data channel asynchronously and without regard to the VDSL Tx_SOC or Rx_SOC signals, i.e., there is no correlation between the Ethernet frame and the SOC signals generated by the VDSL transceiver. Decoupling the Ethernet and VDSL frames provides simplicity whereby the [need to fragment] task of fragmenting the Ethernet frame into multiple VDSL data frames is neither required nor performed. Hence, there is no need to [extract] reassemble the Ethernet frame from the VDSL frames at the receiving station. To maintain protocol robustness in the absence of start of frame sync pulses from the transceiver, the receiving station utilizes a synchronization method to find the start and end of an Ethernet frame. In the event synchronization is lost, this method is used by the receiving station to resynchronize without the lost of an excessive number of frames.

Paragraph beginning on page 23, line 6

The TxCLK signal is driven by the VDSL transceiver. In order for the bytes to traverse from the 10 MHz clock of the data processor to the TxCLK domain, a byte wide FIFO is used. When the Tx buffer in the memory contains at least one complete Ethernet frame, the data processor transfers bytes to the TIPO circuitry over the VDO bus [and] which are then pushed into the FIFO [by] in response to the PUSH signal [generated] output by the data processor. If the FIFO is not full, the

VFD_RDY signal is asserted to indicate to the data processor that it may transmit another byte to the FIFO in the TIPO circuitry.

Paragraph beginning on page 23, line 18

The TIPI circuitry 118 will now be described in more detail. The TIPI circuitry on the VDSL transceiver side functions to receive the VDSL data frames from the VDSL transceiver, i.e., the Broadcom BCM6010 IC, over the byte wide RxData input bus. The VDSL bytes are clocked into the TIPI by the RxCLK [input] signal provided by the VDSL transceiver. An error indication signal Rx_Err provided by the VDSL transceiver is asserted for the duration of an entire VDSL frame length if [the data frame contains] an uncorrectable error in the data frame is detected. When such as event occurs, the TIPI circuitry sets an 'error in frame' flag that is conveyed to the data processor via interrupt means or status register means.

Paragraph beginning on page 25, line 4

A state transition diagram illustrating the state machine implemented in transferring data from the Ethernet In circuitry to the data processor is shown in Figure 9. The state machine, generally referenced 140, functions to transfer the incoming Ethernet frames from the EI circuitry to the memory. The data processor allocates a Tx buffer and controls the memory interface signals: data bus, address bus, WR and OE signals. [The once] Once a second frame is transferred to the memory, the data processor asserts the backpressure signal at least 1 [μs] microsecond prior to the end of the incoming frame. Since the frame length cannot be predicted, it is assumed to be the shortest possible, i.e., 64 bytes. Thus, when the byte count reaches 60, the backpressure signal is asserted.

Paragraph beginning on page 25, line 20

[The] Which Tx buffer the incoming frame is written to depends on the status of the two buffers as indicated in the EI_buffer_status register, which can have the following values:

Paragraph beginning on page 26, line 17

A state transition diagram illustrating the state machine implemented in transferring data from the data processor to the Transport Independent Parallel Out circuitry is shown in Figure 10. This state machine, generally referenced 150, functions to transfer the Ethernet bytes previously stored in the Tx buffer in the memory [and sends them] to the TIPO circuitry for forwarding to the VDSL transceiver. A FIFO within the TIPO circuitry receives the bytes from the data processor.

When this FIFO is full, the VFR_RDY signal is deactivated and the byte transfer process is suspended.

Paragraph beginning on page 27, line 3

The bytes in the Tx buffer begin to be transferred. The frame length is determined from the [6th] sixth and [7th] seventh bytes. The length read is written into a frame_length counter. This counter is decremented on each non-idle access to the memory. When the counter reaches zero, the machine enters the next state, i.e., End of Transfer 156.

Paragraph beginning on page 27, line 18

A diagram illustrating the relationship over time of input to output Ethernet frames and the EI_buffer_status register contents is shown in Figure 11. The contents of the EI_buffer_status is shown in trace 132 along with the backpressure indication 130. A plurality of input and output Ethernet frames 134 are also shown. Note that only the inbound Ethernet frames are spaced apart by the Interframe Gap (IFG) of 9.6 microseconds while the outbound Ethernet frames have no IFG between them while being transmitted over the VDSL channel.

Paragraph beginning on page 28, line 21

In [this] the Fill Ethernet Rx Buffer state, the incoming Ethernet bytes are transferred to one of the Rx buffers. The frame_length counter is incremented. Note that the preamble is stripped off but the length is stored in the buffer. Bytes are transferred until the frame_length counter is equal to the frame length at which point the transfer is complete. Note that bytes are transferred only while the VFR_AVL signal is active. If during the transfer state 168, the Rx_Err signal is asserted, the Wait for Rx_Err to Clear state 162 is entered and the transfer ceases.

In the Abstract:

An apparatus for and method of encapsulating Ethernet frames over a Very high speed Digital Subscriber Line (VDSL) transport facility. The VDSL frames are transmitted over a point to point VDSL link where they are subsequently extracted and forwarded as standard Ethernet frames. The VDSL facility transport system comprises an Ethernet to VDSL Customer Premises Equipment (CPE) coupled to a DSL Access Multiplexor (DSLAM) over a VDSL transport facility. The Ethernet to VDSL CPE functions to receive a 10BaseT Ethernet signal and encapsulate the Ethernet frame into a VDSL frame for transmission over the VDSL facility. The DSLAM is adapted to receive VDSL frames, extract Ethernet frames therefrom and generate and output a standard

Ethernet signal. Ethernet frames are encapsulated within VDSL frames and transmitted on the wire pair without regard to the state of the Tx and Rx SOC signals output by the VDSL transceiver.